ABSTRACT OF THE DISCLOSURE

A semiconductor structure with partially etched gate and method of fabricating the same. A semiconductor structure with a single-sided or dual-sided partially etched gate comprises a gate dielectric layer, a gate conductive layer and a cap layer sequentially stacked on a substrate to form a gate structure, and a lining layer disposed on sidewalls of the gate structure, wherein the lining layer is partially etched to expose the adjacent gate structure. In addition, an inter-layer dielectric layer covers the gate structure and a contact is formed in the inter-layer dielectric layer, exposing the substrate and a portion of the gate structure therein, wherein the lining layer of the exposed portion of the gate structure is partially removed.